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EP 0696851 A1

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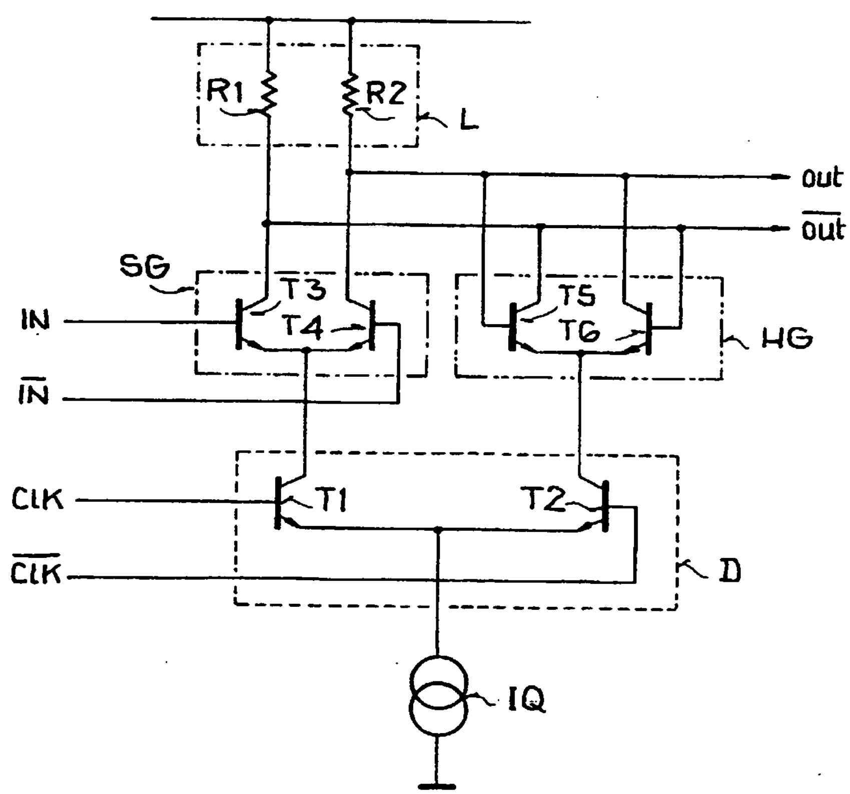
(54) Abstract Title
Method for increasing the cut-off frequency in flip-flops

(57) In a flip-flop comprising a control element SG and a holding element HG, in which a first current causes the control element SG to set a logic state and a second current causes the holding element HG to maintain the logic state, the cutoff frequency is increased by dimensioning the transistors T5, T6 of the holding element HG to be smaller than the transistors T3, T4 of the control element SG.



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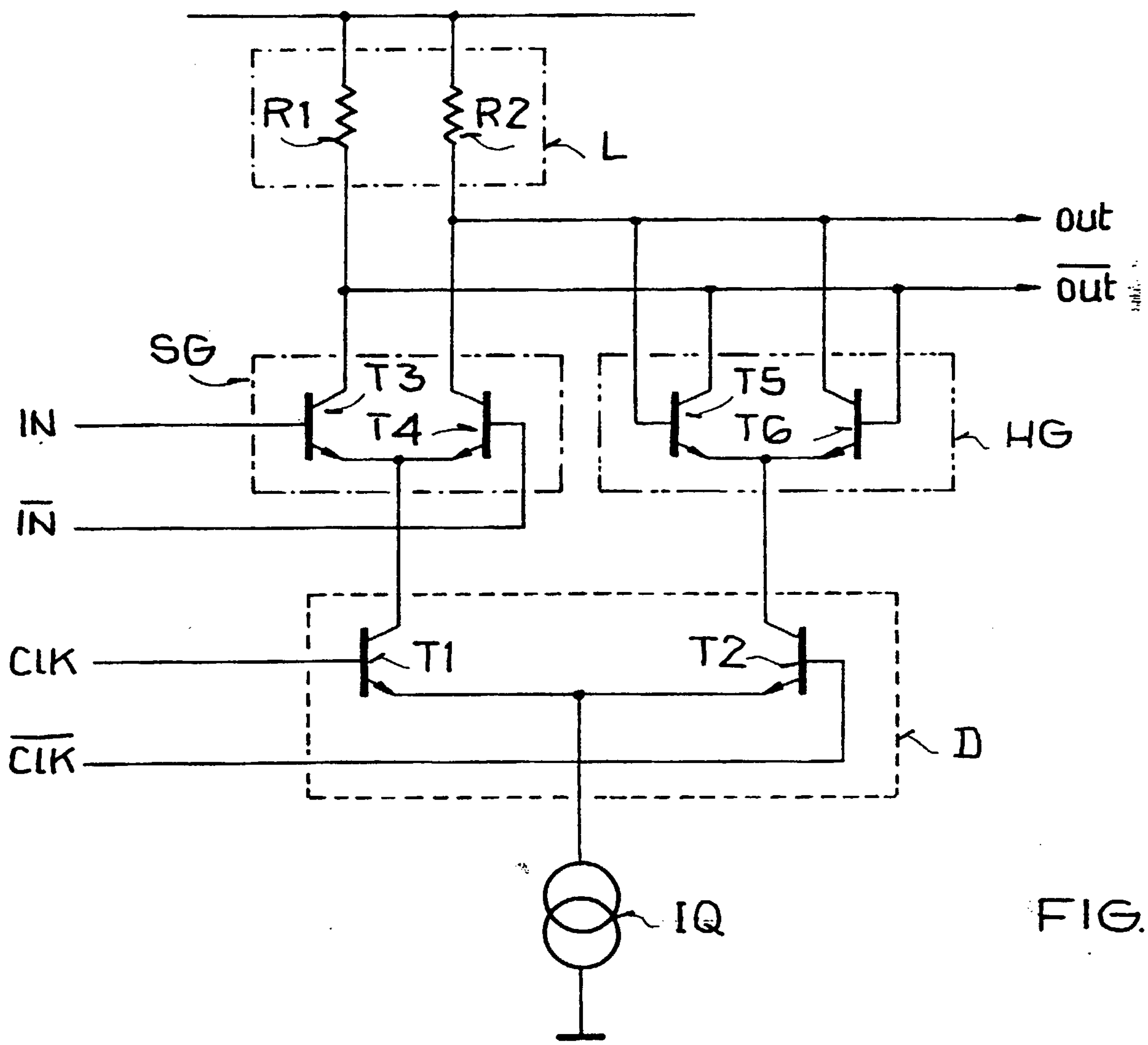
R1
R2
L
out
$\overline{\text{out}}$
SG
T3
T4
T5
T6
HG
IN
$\overline{\text{IN}}$
ClK
$\overline{\text{ClK}}$
T1
T2
D
IQ

FIG.

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Method for increasing the cut-off frequency in flip-flops

The invention relates to a method for increasing the cut-off frequency of flip-flops.

Circuits with flip-flops are used in the digital signal processing field for storing logic states. They consist internally of a control element, which takes the logic state which is applied to its input and makes it available for evaluation at its output, and of a holding element, which maintains the state which is set. Using a clock, inter alia, so-called frequency dividers or dividing stages can be assembled from a series connection of a plurality of flip-flops. The processing of increasingly higher frequencies requires dividing stages which operate at several gigahertz, especially in the GSM, ISM wireless communication field. Because of the development to higher frequencies, the transistors which are used in the flip-flops have to meet higher requirements in terms of the cut-off frequency thereof, which must be approximately twice the maximum frequency of the divider.

The transistor production process is becoming significantly more complex and cost-intensive due to the higher frequency requirements. The cut-off freqüency of an individual flip-flop circuit results from the signal propagation time within the circuit. It is essentially determined by the product of the load resistance and the capacitance at the output line of the flip-flop and, considered quite generally, can be conceived as a low pass filter. With a given load resistance, the transistors of the circuit must be able to handle a sufficiently high current, according to the value of the capacitance which is to be recharged upon a change occurring in the logic state. If this is not the case, high-current effects will occur and the cut-off frequency of the flip-flop drop drastically.

In the methods known from the prior art, for example in M.

Wurzer et. al., ISSCC 2000, San Francisco, the transistors which are used in the control elements and holding elements are dimensioned to prevent high-current effects following the maximum peak current values occurring in the control elements.

The disadvantage of the previous method lies in the fact that the different electrical requirements to be met by the control element and the holding element are not taken into account and the transistor capacitances linked with the area consequently not optimised. As these have to be recharged at the output lines of the flip-flop each time there is a change in the logic state, this has an adverse influence on the cut-off frequency of the flip-flop.

The present invention seeks to provide a method which increases the cut-off frequency of flip-flops and which can at the same time be implemented easily and inexpensively.

According to the present invention, there is provided a method for increasing the cut-off frequency of a flip-flop which comprises at least one control element having at least two transistors and at least one holding element having at least two transistors, and the control element sets by means of a first current a logic state of the flip-flop which is maintained by the holding element by means of a second current, wherein the current carrying capacity of the transistors of the control element is adapted to the value of the first current, and the current carrying capacity of the transistors of the holding element is adapted to the value of the second current.

Methods according to embodiments of the invention relate to adapting the current carrying capacity of the transistors of a holding element in a flip flop separately from the current

carrying capacity of a control element. The task of the control element is to transfer the logic state which is applied to an input to an output of the flip-flop by means of a first current.

If the logic state at the input changes, there will also be a change in the value of the first current at the output. It is of advantage if the current in this case produces via a load element a voltage drop which corresponds to the logic states. The task of the holding element is to maintain the logic state which is set by the control element by means of a second current. If the logic state at the input of the control element corresponds to the state already existing at the output, the two currents will be equal, i.e. the requirement in terms of the value of the current carrying capacity of the transistors of the control element and the transistors of the holding element will be equal in static operating mode. If the logic state changes at the input, the value of the first current must be changed by the control element. This means that the capacitances which are present at the output of the control element must be recharged by the transistors of the control element in dynamic operating mode. An additional current is required for this when compared with the static operating mode. The current carrying capacity of the transistors of the control element must therefore be greater than the current carrying capacity of the transistors of the holding element. As the value of the current carrying capacity in the transistors is proportional to the capacitance thereof, the contribution of the transistors to the capacitance at the output of the flip-flop is reduced when compared with the prior art and the cut-off frequency is increased as a result.

The required current carrying capacity is preferably calculated by means of simulation of the circuit parts before

the circuit is produced. The requirements in terms of current carrying capacity are in this case implemented by dimensioning the transistors during the layout phase, preferably by means of scaling the area of the transistor types which are used for a flip-flop circuit arrangement. According to the purely static requirements, the transistors of the holding element have smaller dimensions than the transistors of the control element. As the specific transistor capacitances are proportional to the transistor area, the reduction in the transistor area results in a reduction in the capacitance with respect to the prior art. A further advantage lies in the fact that the chip area can be reduced when producing an integrated flip-flop circuit arrangement by means of a smaller transistor area.

A preferred embodiment of the present invention will now be explained, by way of example only. The invention is explained in the following on the basis of in connection with the drawing, in which:

Figure 1 is a block diagram showing an embodiment of a flip-flop.

The task of the flip-flop circuit arrangement which is illustrated in Figure 1 is to store the digital state which is applied to an input IN, $\overline{IN}$ and make this state available at an output, OUT, $\overline{OUT}$ for further processing. For this purpose the flip-flop comprises a current source IQ, which lies between a reference potential and a clock element D. The clock element D is also connected to a control element SG and a holding element HG and comprises an input CLK and a complementary input $\overline{CLK}$. In addition to the input IN and the complementary input $\overline{IN}$, the control element SG also comprises the output OUT and the complementary output $\overline{OUT}$. Each of the two outputs OUT

and $\overline{OUT}$ is separately connected via a resistor R1 and a resistor R2 of a load element L to a supply potential and to a first terminal and a second terminal of the holding element HG.

In the illustrated embodiment the clock element D comprises a first transistor T1 and a second transistor T2, the emitters of which are jointly connected to the current source IQ. The base of the transistor T1 is connected to the input CLK and the base of the transistor T2 to the input $\overline{CLK}$. The collector of the transistor T1 is also connected to the two emitters of a first transistor T3 and a second transistor T4 of the control element SG. The collector of the transistor T2 is accordingly connected to the two emitters of a transistor T5 and a transistor T6 of the holding element HG. In the control element SG the base of the transistor T3 is connected to the input IN and the base of the transistor T4 to the input $\overline{IN}$, while the collector of the transistor T3 is connected to the output $\overline{OUT}$ and the collector of the transistor T4 to the output OUT. In the holding element HG the base of the transistor T5 and the collector of the transistor T6 are connected to the output line OUT and the base of the transistor T6 and the collector of the transistor T5 jointly to the output line $\overline{OUT}$.

The clock element 10 forms the starting point for the functional description. This decouples the current source IQ from the control element SG and the holding element HG. If the input CLK is at "low", the entire current will flow through the holding element HG, as the input CLK is at "high".

The entire current accordingly flows through the control element SG while the input CLK is "high". Because of the "high" potential at the input CLK, the control element SG

becomes transparent, i.e. the respective logic state which is applied to the input IN is reproduced inverted on the output line $\overline{OUT}$ through a voltage drop at the load element L. If there is a change in potential from "high" to "low" at the input CLK, the holding element HG will take the logic state which is set by the control element SG.

As the current of the current source IQ flows either entirely through one of the transistors T3 and T4 of the control element SG or through one of the transistors T5 and T6 of the holding element HG in static mode, the four transistors T3 to T6 must have the same current carrying capacity for the static mode. In contrast, a change of potential to be carried out by the transistors T3 and T4 of the control element SG at the outputs OUT and $\overline{OUT}$ can only be described by means of a dynamic mode of observation. According to the change in direction of the logic state, either the transistor T3 or the transistor T4 must for this purpose recharge the respective capacitance at the output lines OUT and $\overline{OUT}$, while the transistors T5 and T6 of the holding element HG do not bring about any change and are therefore to be considered as purely static. However the geometry of the transistors T3 and T4 must therefore be enlarged in order to handle the current peaks which occur upon changing the logic state and are proportional to the value of the capacitances present at the output lines OUT and $\overline{OUT}$. In this case the respective capacitance consists of the capacitances of the conductor tracks, the capacitance of the load resistor L, the internal junction capacitances of the transistors T3 to T6, as well as the input capacitance of the follower stage connected to the output line OUT or the output line $\overline{OUT}$. If only the transistors T3 and T4 of the control element SG are enlarged in order to fulfil the dynamic requirements, the additional contribution to the internal transistor capacitances will be reduced to half with respect

to the prior art. As the signal propagation time through the flip-flop is proportional to the product of the total capacitance and the value of the load resistor L, the cut-off frequency of the flip-flop will therefore increase or, at a predetermined frequency, the current consumption of the flip-flop will decrease with respect to the prior art.

Tests carried out by the applicants produced an increase in the cut-off frequency in a flip-flop circuit in the range of 10%. In terms of dividing stages operating, for example, in the range of 5 GHz, the result is an increase in cut-off frequency of 500 MHz. Here the transistors which have a higher internal specific transistor capacitance also exhibit a greater increase in cut-off frequency.

Thus, in summary, whereas in known methods, the area of the transistors is determined in a flip-flop circuit according to the current peaks at the control elements and this area is applied to the transistors of the holding element, according to the present method the area of the transistors of the holding element is adapted to their static current load. As the static current load is smaller than the dynamic current load of the transistors of the control element, the area of the transistors of the holding element is reduced. The total capacitance, which is to be recharged by the transistors of the control element upon a change occurring in the logic state, is therefore reduced. The cut-off frequency of the flip-flop circuit is increased accordingly.

Claims

1. A method for increasing the cut-off frequency of a flip-flop which comprises at least one control element having at least two transistors and at least one holding element having at least two transistors, and the control element sets by means of a first current a logic state of the flip-flop which is maintained by the holding element by means of a second current, wherein the current carrying capacity of the transistors of the control element is adapted to the value of the first current, and the current carrying capacity of the transistors of the holding element is adapted to the value of the second current.

2. A method according to Claim 1, wherein the current carrying capacity of the transistors is adapted by dimensioning the transistors.

3. A method according to Claim 1 or 2, wherein the transistors of the holding element have smaller dimensions than the transistors of the control element.

4. A method substantially as herein described with reference to the accompanying drawings.

5. A flip-flop produced by a method according to any preceding claim.

6. A flip-flop comprising at least one control element having at least two transistors and at least one holding element having at least two transistors, means for supplying a first current to the control element so that it sets a logic state of the flip-flop and a second current to the holding element

so that it maintains the logic state, wherein the transistors of the holding element have smaller dimensions than the transistors of the control element.

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Application No: GB 0119452.1
Claims searched: 1 - 6

Examiner: Brian Mc Cartan
Date of search: 4 February 2002

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.T): H3P (PABMS, PABXX)

Int Cl (Ed.7): H03K (3/012, 3/0233, 3/286, 3/288, 3/289)

Other: ONLINE: WPI, EPODOC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	EP 0696851 A1 (IBM) Column 5, line 33 onwards.	-

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.